THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JAE-SUNG SHIM

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Appeal No. 96-3234
Application 08/184,446[1]

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HEARD: July 15, 1999

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Before KRASS, FLEMING, and BARRY, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

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[1] Application for patent filed January 21, 1994.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 13, all of the claims present in the application.

The invention relates to an error correcting memory system. In particular, on page 3 of the specification, Appellant discloses that the principal object of the present invention is to provide an error correcting memory device for an effective use of the space thereof. Appellant discloses that this object is accomplished by providing an error correcting memory device that includes a device for writing and reading m-bit data and an n-bit pointer for marking errors in accordance with a predetermined rule. The device includes a first memory for recording m-bit data and a second memory for recording n-bit pointers. The device further includes a writing/reading control signal generating unit for generating the respective writing and reading control signals of the first

and second memory so that the m-bit data is stored in the first memory and the n-bit pointer is stored in the second memory.

Independent claim 1 is reproduced as follows:

1. An error correcting memory system which writes and reads m-bit data and an error marking n-bit pointer by a predetermined rule, comprising:

a first memory for recording said m-bit data;

a second memory for recording said n-bit pointer;

an address generating unit for generating the address signals of said first and second memories by a predetermined rule; and

a writing/reading control signal generating unit for generating the respective writing and reading control signals of said first and second memories by receiving the writing and reading control signals and responding to a data/pointer differentiating signal,

wherein m and n are integers greater than or equal to one.

The Examiner relies on the following reference:

Ozaki et al. (Ozaki)	4,719,628	Jan. 12, 1988

Claims 1 through 13 stand rejected under 35 U.S.C. § 112, first paragraph, as being based upon a nonenabling

disclosure. Claims 1 through 4 and 7 through 12 are rejected under 35 U.S.C. § 103 as being obvious over Ozaki.

Rather than repeat the arguments of Appellant or the Examiner, we make references to the briefs[2] and the answer for the details thereof.

OPINION

After a careful review of the evidence before us, we do not agree with the Examiner that Appellant's specification is properly objected to under 35 U.S.C. § 112, first paragraph, for failing to provide an enabling disclosure, and claims 1 through 13 are properly rejected under 35 U.S.C. § 112, first paragraph. In addition, we do not agree with the Examiner that claims 1 through 4 and 7 through 12 are properly rejected under 35 U.S.C. § 103 as being obvious over Ozaki.

[2] Appellant filed an appeal brief on February 9, 1996. Appellant filed a reply brief on May 20, 1996. The Examiner responded to the reply brief on December 24, 1996, thereby entering the reply brief into the record.

In order to comply with the enablement provision of 35 U.S.C. § 112, first paragraph, the disclosure must adequately describe the claimed invention so that the artisan could practice it without undue experimentation. ***In re Scarbrough***, 500 F.2d 560, 566, 182 USPQ 298, 303 (CCPA 1974); ***In re Brandstadter***, 484 F.2d 1395, 1404, 179 USPQ 286, 293 (CCPA 1973); and ***In re Gay***, 309 F.2d 769, 774, 135 USPQ 311, 316 (CCPA 1962). If the Examiner had a reasonable basis for questioning the sufficiency of the disclosure, the burden shifted to the Appellants to come forward with evidence to rebut this challenge. ***In re Doyle***, 482 F.2d 1385, 1392, 179 USPQ 227, 232 (CCPA 1973), ***cert. denied***, 416 U.S. 935 (1974); ***In re Brown***, 477 F.2d 946, 950, 177 USPQ

691, 694 (CCPA 1973); and ***In re Ghiron***, 442 F.2d 985, 992, 169 USPQ 723, 728 (CCPA 1971). However, the burden was initially upon the Examiner to establish a reasonable basis for questioning the adequacy of the disclosure. ***In re Strahilevitz***, 668 F.2d 1229, 1232, 212 USPQ 561, 563 (CCPA

1982); ***In re Angstadt***, 537 F.2d 498, 504, 190 USPQ 214, 219 (CCPA 1976); and ***In re Armbruster***, 512 F.2d 676, 677, 185 USPQ 152, 153 (CCPA 1975). The Examiner points out that the claims recite "a predetermined rule." The Examiner argues that the specification does not disclose the nature of the predetermined rule or how one would be able to make a device that operates according to a predetermined rule.

Appellant provides Watkinson, a prior art reference, which shows examples of expressions used in interleaving blocks of error-encoded CD data. In the reply brief on page 3, Appellant argues that the reference provides an example of the arrangement of data blocks constructed in accordance with sample expressions. Appellant further points out that Watkinson clearly states that P (C1) and Q (C2) redundancy symbols used as pointers are calculated by a known method of polynomial division.

Appellant argues that one of ordinary skill in the art can make and use the recited address generating unit based upon "a

predetermined rule" for error correction and interleaving block code for a compact disk medium. Upon reviewing Watkinson, as well as appellant's specification, we agree that one of ordinary skill in the art would have been able to make and use the recited address generating unit based upon "a predetermined rule" for error-corrected and interleaving block code for a compact disk medium. In particular, we note that the prior art Watkinson clearly shows that the redundancy symbols are calculated by a predetermined rule, in particular, polynomial division. Furthermore, we note that the Appellant's invention is not related to the development of a new predetermined rule. The specification makes clear that the invention is to be used using known error correction detection methods and that the invention is directed to saving memory space using these methods. Therefore, we will not sustain the Examiner's rejection of claims 1 through 13 under 35 U.S.C. § 112, first paragraph.

Claims 1 through 4 and 7 through 12 are rejected under 35 U.S.C. § 103 as being obvious over Ozaki. On page 2 of the Examiner's answer, the Examiner states that the

Examiner's position is set forth in Paper No. 4. Turning to Paper No. 4,

the Examiner states that the admitted prior art in Appellant's specification on pages 1 through 3 shows that there are 8 bit data and a one bit pointer. The Examiner argues that the memory is arranged to store by byte so that the pointer is stored in a byte location thereby wasting the other 7 bits. The Examiner argues that Ozaki discloses a system where the pointer memory is equal to the number of bits of the pointer.

Appellant argues on page 23 of the appeal brief that the admitted prior art and Ozaki fail to teach a writing/reading control signal generating unit for generating the respective writing and reading control signals of first and second memories by receiving the writing and reading control signals and responding to a data point differentiating signal as recited in claim 1. On page 27 of the appeal brief, Appellant argues that the admitted prior art and Ozaki fail to teach or suggest a data bus driving unit for driving an m + n bit data bus operatively connected to said memory bi-

directionally by dividing said m + n bit data into m-bits and n-bits in response to a data input control signal and pointer writer control signal as recited in claim 3.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assoc., Inc. v. Garlock, Inc.***, 721 F.2d

1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied,*** 469 U.S. 851 (1984). Finally, the Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

Upon a careful review of the admitted prior art and Ozaki, we fail to find that either of these references teaches or suggests the above claim limitations as recited in Appellant's independent claims 1 and 3. Neither the admitted prior art nor Ozaki recognizes the problem of saving memory due to the fact that only one bit needs to be stored and the de-interleaving of the data being received. Furthermore, neither reference teaches or suggests a writing/reading control signal generating unit which allows the m-bit data to be stored in a first memory and the n-bit pointer to be stored

in the second memory as claimed in Appellant's claim 1. Furthermore, neither reference teaches or suggests a data bus driving unit for driving an m + n bit data bus operatively connected to a memory whose capacity is m + n bits bi-directionally by dividing said m + n bit data into m-bits and n-bits in response to a data input control signal and a pointer writing control signal as recited in Appellant's independent claim 3. Therefore, we will not sustain the Examiner's rejection of claims 1 through 4 and 7 through 12 under 35 U.S.C. § 103 as being obvious over Ozaki.

Therefore, we have not sustained the rejection of claims 1 through 13 under 35 U.S.C. § 112, first paragraph, or the rejection of claims 1 through 4 and 7 through 12 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

MRF:psb

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